In re David Glen Roe
Application No. 09/814,244

REMARKS

Claims 1, 9, 15, 18, and 20 (all five pending independent claims) stand rejected under 35 USC 103(a) as being obvious over Kicuchi, US. Patent 5,977,806.

Applicants traverse these rejections as the Office action fails to establish a primia facie case of obviousness as Kicuchi neither teaches nor suggests all the claim elements and limitations as required by the MPEP. The burden is on the Office action to establish a prima facie case of obviousness, which has not been done as the MPEP requires, *inter alia*, that:

> "the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure."

MPEP § 706.02(j) (*citing In re Vaeck*, 947 F.2d 488 (Fed. Cir. 1991))(emphasis added).

First:

- claim 1 recites a circuit comprising "... a first phase-locked loop circuit including: an off-chip reference clock input, a first set of one or more phase-locked loop clock outputs, and a buffered reference clock output...";
- claim 9 recites the circuit comprising "... means for buffering a received off-chip reference clock signal electrically coupled between the off-chip reference clock input and the buffered reference clock output...";
- claim 15 recites a method comprising: "... selecting a first phase-locked loop macro including an off-chip reference clock input, a first set of one or more phase-locked loop clock outputs, and a buffered reference clock output...";
- claim 18 recites a method comprising: "... generating, by the first phase-locked loop circuit, a buffered reference clock signal and the first set of internal clock reference signals..."; and

- claim 20 recites a system comprising: "... means for generating, by the first phase-locked loop circuit, a buffered reference clock signal and the first set of internal clock reference signals" (emphasis added).

Kikuchi neither teaches nor suggests these elements, and thus, the Office action fails to present a prima facie case of obviousness as required by the MPEP.

Additionally, the Office action apparently examines claim 1, but fails to address claim elements/limitations of each and every claim as required by the MPEP, the Office action hand-waves by saying "[t]he same applies to claims 9, 15, 18, and 20", which have different elements/limitations which are not addressed by the Office action in contrast the requirements of a proper rejection pursuant to the MPEP. For example, claim 15 references first and second phase-locked loop macros, and Kikuchi neither teaches nor suggests such macros, nor other claim limitations, and thus is not a proper § 103 rejection.

Applicant agrees with the compound statement in the Office action that "Kikuchi does not disclose a buffered reference clock output of the first phase-locked loop (10) being electrically coupled to the on-chip reference clock input of the second phase-locked loop circuit (54)." However, the Office action ignores that facts that (a) Kikuchi does not even have a buffered reference clock output, and (b) Kikuchi neither teaches nor suggests first phase-locked loop (10) including a buffered reference clock output. Additionally, the Office action relies on FIG. 1 for teaching an off-chip reference clock input for the first PLL and an off-chip reference clock input, yet FIG. 1 shows they are connected, apparently electrically connected, so they're both the same - i.e., both being off-chip reference clock inputs which is not what is recited in claim 1.

The MPEP requires the prior art reference(s) used in a proper 103 rejection to include all elements and limitations. For at least these reasons, the Office action fails to present a prima facie case of obviousness in accordance with the MPEP for all pending independent claims.

Moreover, for at least the reasons presented herein in relation to Paragraph 3, the Office action fails to make a prima facie case of anticipation nor obviousness in regards to all pending

independent claims, and thus, all pending claims (claims 1-20) are believed to be allowable as the rejections in relation to Paragraph 4 rely on such a prima facie case being established.

Applicant believes its requirements for responding to the Office action under 37 CFR § 1.111 have been satisfied, but to help further advance this application this along, the Kikuchi reference will be discussed further. First, all independent claims and FIG. 1 (on which the Office action relies in its rejection of all claims) of Kikuchi teach that the "the input signal of said first PLL circuit is used as the reference signal of said second PLL circuit."

However, Kikuchi further teaches that the reference signal for the second PLL circuit can be different than that of the first PLL circuit or if it is the same, there a signal generation source can be omitted. Specifically, Kikuchi recites in col. 8. ll. 7-14:

> "Furthermore, in each of the above-described embodiments, as a reference signal for the second PLL circuits 20, 50 and 80, a signal is used which is different from the input signal of the first PLL circuit 10, 40 and 70. However, it is also possible to use the input signal of the first PLL circuits 10, 40 and 70 as it is. This makes it possible to omit a signal generation source exclusively used for generating a reference signal." (Emphasis added.)

This further supports that Kikuchi neither teaches nor suggests the first phase-locked loop having a buffered reference clock output, nor means for buffering a received off-chip reference clock signal, nor generating a buffered reference clock signal, nor means for generating a buffered reference clock signal as recited in independent claims 1, 9, 15, 18, and 20.

Once again, Applicant agrees with the July 17, 2002, Office action that the "IBM reference does not disclose that the buffered reference clock output (BUFREFCLK) of the first phase-locked loop circuit is electrically coupled to the on-chip reference clock input (REFCLK) of the second phase-locked loop circuit (PLL7SLIBI)." Moreover, applicants submit that the IBM reference teaches away from such a combination as recited in independent claim 1. The IBM Reference, at least on page 843, teaches that the REFCLK of PLL7SLIBI "typically connects to the output of a receiver. Any receiver in the library may be used (differential or single-ended) provided that it is located in a test I/O slot." In other words, the IBM reference teaches that the REFCLK of PLL7SLIBI is connected to an I/O receiver (e.g., for receiving an

off-chip signal), and not to another component, such as BUFREFCLK of a first phase-locked loop circuit.

Kikuchi provides no teaching to overcome this deficiency. Rather Kikuchi is consistent with this teaching away from the combinations recited in independent claims 1, 9, 15, 18, and 20. Based on all claims and FIG. 1 of Kikuchi, the combination of Kikuchi with the IBM reference (even if there was such a teaching to combine these references) produces a circuit with the on-chip reference clock input of a second phase-locked circuit *coupled to the input signal of the first phase locked loop.* In contrast, claims 1-20 require the on-chip reference clock input of a second phase-locked loop circuit to be *coupled to the buffered reference clock output of a first phase-locked loop circuit.* For at least this reason, Kikuchi nor the IBM reference, alone or in combination, neither teaches nor suggests the invention recited in claims 1-20.

For at least these reasons, applicants request the rejections of claims 1-20 be withdrawn, and claims 1-20 be allowed.

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CONCLUSION

In view of the above remarks, the application is considered in good and proper form for allowance, and the Examiner is respectfully requested to pass this application to issue. If, in the opinion of the Examiner, a telephone conference would expedite the prosecution of the subject application, the Examiner is invited to call the undersigned attorney.

The Commissioner is hereby generally authorized under 37 C.F.R. § 1.136(a)(3) to treat this communication or any future communication in this or any related application filed pursuant to 37 C.F.R. § 1.53 requiring an extension of time as incorporating a request therefore, and the Commissioner is hereby specifically authorized to charge Deposit Account No. 501430 for any fee that may be due in connection with such a request for an extension of time.

The Commissioner is hereby authorized to charge payment of any fee due any under 37 C.F.R. §§ 1.16 and § 1.17 associated with this communication or any future communication in this or any related application filed pursuant to 37 C.F.R. § 1.53 or credit any overpayment to Deposit Account No. 501430.

Respectfully submitted,
The Law Office of Kirk D. Williams

Date: September 17, 2003

By [signature] 9/17/03

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